CLAIMS

What is claimed is:

1. A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices;

memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device; and

a self-test module coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range, the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals.

2. The memory module of claim 1 wherein the memory hub further comprises an externally accessible maintenance port operable to provide access to signals indicative of whether the at least one memory device properly responded to the first and second signals.

3. The memory module of claim 1 wherein the memory hub further comprises a plurality of link interfaces, a plurality of memory device interfaces, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

4. The memory module of claim 1 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

5. The memory module of claim 1 wherein the self-test module further comprises:

a pattern generator producing a pattern of data bits each of which is used to generate a respective one the first signals in the series; and

a comparator coupled to the pattern generator and to the at least one memory device, the comparator receiving output signals from the at least one memory device and determining a pattern of data corresponding thereto, the comparator further and comparing the pattern generated from the output signals to the pattern of data from which the first signals are generated.

6. The memory module of claim 1 wherein the self-test module further comprises a storage device coupled to the comparator to store the results of the comparisons between the pattern generated from the output signals and the pattern of data from which the first signals are generated.

7. The memory module of claim 1 wherein the self-test module comprises:

a delay line receiving a clock signal that is synchronized to the second signals in the series, the delay line generating from the clock signal a respective internal

clock signal that is used to control the timing of when each of the first signals in the series is coupled to the at least one memory device;

a memory sequencer coupled to the at least one memory device, the memory sequencer generating and coupling to at least one memory device a sequence of control signals to cause the at least one memory device to respond to each of the first and second signals in the series; and

a built-in self-test engine coupled to the delay line and to the memory sequencer for controlling the delay of the delay line.

8. The memory module of claim 7 wherein the self-test module further comprises a flip-flop having a data input receiving each of the first signals in the series, a clock input receiving the internal clock signal, and an output coupled to the at least one memory device.

9. The memory module of claim 1 wherein each of the first signals comprises a data signal and each of the second signals comprise a data strobe signal.

10. The memory module of claim 1 wherein the self-test module is further operable to couple a signal from the memory device corresponding to each of the output signals and to alter the relative timing between the signal coupled from the memory device and the corresponding output signal.

11. A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices;

memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device; and

a self-test module coupled to at least one of the memory devices, the self-test module being operable to receive first and second signals from the at least one memory device, the self-test module being operable to alter the relative timing between when some of the corresponding first and second signals in the series are coupled from the at least one memory device over a range and to evaluate the operation of the least one memory device based on the first and second signals.

12. The memory module of claim 11 wherein the memory hub further comprises an externally accessible maintenance port operable to provide access to signals indicative of the evaluation of the operation of the least one memory device.

13. The memory module of claim 11 wherein the memory hub further comprises a plurality of link interfaces, a plurality of memory device interfaces, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

14. The memory module of claim 11 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

15. The memory module of claim 11 wherein the self-test module further comprises a storage device operable to store the evaluations of the operation of the least one memory device.

16. The memory module of claim 11 wherein the self-test module comprises:

a delay line receiving each of the first signals in the series, the delay line generating from each of the first signals a respective delayed first signal that is used to evaluate the operation of the least one memory device;

a memory sequencer coupled to the at least one memory device, the memory sequencer generating and coupling to at least one memory device a sequence of control signals to cause the at least one memory device to respond to each of the first and second signals in the series;

a built-in self-test engine coupled to the delay line and to the memory sequencer for controlling the timing of each of the delayed first signals relative to the corresponding second signal.

17. The memory module of claim 16 wherein the self-test module further comprises a flip-flop having a data input receiving each of the second signals in the series, a clock input receiving the delayed clock signal, and an output producing a signal that is used to evaluate the operation of the at least one memory device.

18. The memory module of claim 11 wherein each of the first signals comprises a data strobe signal and each of the second signals comprise a data signal.

19. A memory module, comprising:

a plurality of synchronous memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices;

memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device; and

a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal; and

a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range, the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied.

20. The memory module of claim 19, wherein the self-test module further comprises:

a delay line receiving the clock signal from the variable frequency clock generator and generating a delayed internal clock signal; and

a flip-flop having a data input coupled to receive the first signal, a clock input coupled to receive the internal clock signal, and an output coupled to the at least one memory device.

21. The memory module of claim 19 wherein the memory hub further comprises an externally accessible maintenance port operable to provide access to signals indicative of whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied.

22. The memory module of claim 19 wherein the memory hub further comprises a plurality of link interfaces, a plurality of memory device interfaces, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

23. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface coupled to the system memory port for receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data

to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device; and

a self-test module coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range, the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals.

24. The processor-based system of claim 23 wherein the memory hub further comprises an externally accessible maintenance port operable to provide access to signals indicative of whether the at least one memory device properly responded to the first and second signals.

25. The processor-based system of claim 23 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

26. The processor-based system of claim 23 wherein the self-test module further comprises:

a pattern generator producing a pattern of data bits each of which is used to generate a respective one the first signals in the series; and

a comparator coupled to the pattern generator and to the at least one memory device, the comparator receiving output signals from the at least one memory device and determining a pattern of data corresponding thereto, the comparator further

and comparing the pattern generated from the output signals to the pattern of data from which the first signals are generated.

27. The processor-based system of claim 23 wherein the self-test module further comprises a storage device coupled to the comparator to store the results of the comparisons between the pattern generated from the output signals and the pattern of data from which the first signals are generated.

28. The processor-based system of claim 23 wherein the self-test module comprises:

a delay line receiving a clock signal that is synchronized to the second signals in the series, the delay line generating from the clock signal a respective internal clock signal that is used to control the timing of when each of the first signals in the series is coupled to the at least one memory device;

a memory sequencer coupled to the at least one memory device, the memory sequencer generating and coupling to at least one memory device a sequence of control signals to cause the at least one memory device to respond to each of the first and second signals in the series; and

a built-in self-test engine coupled to the delay line and to the memory sequencer for controlling the delay of the delay line.

29. The processor-based system of claim 28 wherein the self-test module further comprises a flip-flop having a data input receiving each of the first signals in the series, a clock input receiving the internal clock signal, and an output coupled to the at least one memory device.

30. The processor-based system of claim 23 wherein each of the first signals comprises a data signal and each of the second signals comprise a data strobe signal.

31. The processor-based system of claim 23 wherein the self-test module is further operable to couple a signal from the memory device corresponding to each of the output signals and to alter the relative timing between the signal coupled from the memory device and the corresponding output signal.

32. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of synchronous memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling

read memory requests to the memory device and coupling read data from the memory device; and

a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal; and

a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range, the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied.

33. The processor-based system of claim 32, wherein the self-test module further comprises:

a delay line receiving the clock signal from the variable frequency clock generator and generating a delayed internal clock signal; and

a flip-flop having a data input coupled to receive the first signal, a clock input coupled to receive the internal clock signal, and an output coupled to the at least one memory device.

34. The processor-based system of claim 32 wherein the memory hub further comprises an externally accessible maintenance port operable to provide access to signals indicative of whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied.

35. The processor-based system of claim 32 wherein the memory hub further comprises a plurality of link interfaces, a plurality of memory device interfaces, and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces.

36. A method for performing signal timing testing on memory system having a memory hub coupled to a plurality of memory devices, the method comprising:

generating testing signals in the memory hub;

coupling the testing signals from the memory hub to the memory devices while varying the relative timing between when the testing signals are applied to the memory devices.

generating output signals in the memory devices resulting from the testing signals;

coupling the output signals from the memory devices to the memory hub;

evaluating the output signals in the memory hub to determine if the memory devices properly responded to the test signals.

37. The method of claim 36 wherein the testing signals comprise data signals and corresponding data strobe signals.

38. The method of claim 37 wherein the act of generating testing signals in the memory hub comprises:

generating a pattern of data:

storing the pattern of data: and

producing write data bit signals from the data pattern.

39. The method of claim 38 wherein the act of generating output signals in the memory devices resulting from the testing signals comprise generating read data bit signals.

40. The method of claim 39 wherein the act of evaluating the output signals in the memory hub comprises:

determining a data pattern corresponding to the read data bit signals received from the memory devices; and

comparing the data pattern corresponding to the read data bit signals to the stored pattern of data.

41. The method of claim 36 wherein the testing signals comprise command signals and a clock signal.

42. A method for performing signal timing testing on memory system having a memory hub coupled to a plurality of memory devices, the method comprising:

in the memory hub, generating write data and a data strobe signal for each of a plurality of write memory operations;

storing the write data in the memory hub;

coupling the write data and the data strobe signal for each of the plurality of write memory operations from the memory hub to the memory devices while altering

the relative timing between the write data and the data strobe signal in at least some of the write memory operations;

in the memory devices, storing the write data coupled from the memory hub;

reading the write data stored in the memory devices by coupling read data from the memory devices to the memory hub in each of a plurality of read data operations; and

in the memory hub, comparing the read data coupled from the memory devices to the write data coupled to the memory devices.

43. The method of claim 42, further comprising:

coupling a read data strobe from the memory devices to the memory hub along with the read data;

in the memory hub, altering the relative timing between when the read data and the read data strobe signal are registered in the memory hub in at least some of the write memory operations; and

comparing the registered read data coupled from the memory devices to the write data coupled to the memory devices.

44. A method for performing signal timing testing on memory system having a memory hub coupled to a plurality of memory devices, the method comprising:

in the memory hub, generating a memory command and a clock signal for each of a plurality of memory operations;

coupling the memory command and the clock signal for each of the plurality of memory operations from the memory hub to the memory devices while altering the relative timing between the memory command and the clock signal in at least some of the memory operations;

in the memory devices, performing a memory operation for each of the plurality of memory commands;

reading the data from the memory devices by coupling read data from the memory devices to the memory hub in each of a plurality of read data operations; and

in the memory hub, determining if the memory devices properly performed the memory operations corresponding to the memory commands based on the read data.

45. A method for performing signal timing testing on memory system having a memory hub coupled to a plurality of memory devices, the method comprising:

in the memory hub, generating a clock signal having a variable frequency;

coupling test signals and the clock signal for each of a plurality of memory operations from the memory hub to the memory devices while altering the frequency of the clock signal in at least some of the memory operations;

in the memory devices, responding to the test signals coupled from the memory hub;

reading data stored in the memory devices by coupling read data from the memory devices to the memory hub in each of a plurality of read data operations; and

in the memory hub, determining from the read data coupled from the memory devices whether the memory devices properly performed the memory operations.

46. The method of claim 45 wherein the memory operations comprise write memory operations.

47. The method of claim 46 wherein the test signals comprise write data signals.

48. The method of claim 46 wherein the test signals comprise command signals.

49. The method of claim 45 wherein the memory operations comprise read memory operations.

50. The method of claim 49 wherein the test signals comprise command signals.